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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/394,564	09/10/1999	HOWARD THOMAS OLNOWICH	EN997080B	4402

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IBM Corporation  
Intellectual Property Law (Dept. 917, Bldg. 006-1  
3605 Highway 52 North  
Rochester, MN 55901-7829

EXAMINER

BATAILLE, PIERRE MICHE

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 03/15/2004

25

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/394,564

Applicant(s)

OLNOWICH, HOWARD THOMAS

Examiner

Pierre-Michel Bataille

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-49 is/are pending in the application.
- 4a) Of the above claim(s) 2-30 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1 and 31-39 is/are allowed.
- 6) ☒ Claim(s) 40-49 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Amendment***

1. This Office Action is taken in response to Applicant Request For Continuing Examination (RCE) filed February 2, 2004. Applicant's amendment and/or arguments have been considered with the results that follow.

### ***Response to Arguments***

2. Applicant's arguments with respect to claims 40-49 have been considered but are moot in view of the new ground(s) of rejection.

The previous rejection in view of US Patent No. 6,249,520 (Steely, Jr. et al) has been withdrawn as the instant application claims priority of US Application 08/890,341 filed July 10, 1997 which is before the filing date of the applied reference by Steely Jr. However, a new reference is applied against claims 40-49 as the new reference, having an effective filing date of June 7, 1995, anticipates the claimed invention. New Ground of rejection follows.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 40-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,049,889 (Steely, Jr. et al).

With respect to claims 40-44, Steely, jr. discloses, as required in the claims, an interconnect for parallel computing in a multiprocessing system including a plurality of processing nodes (nodes 12-14-16-18, Fig. 1) which allows coherency of a data structure between said plurality of processing nodes in a cluster to be maintained [Col. 4, Lines 30-34; Col. 7, Line 55 to Col. 8, Line 2]; a multi-stage communication network for interconnecting said processing nodes (MC HUB 21); each processing node including a unique section of shared memory which is not a cache (local address space; Col. 3, Lines 64-67);

a cache coherency directory is distributed to each of said node for tracking which of said nodes have a copy of each cache line (control structure for each item of the memory data to be shared by the plurality of nodes wherein the control structure includes a number of entries corresponding to a number of nodes for each item of the memory data to be shared by the plurality of nodes) [Col. 2, Lines 26-28] and

an adapter (adapter disposed between the memory and the interconnect) for storing changed data immediately to said unique section of shared memory regardless of which of said node is changing the data and which of said nodes includes the section of shared memory to be changed, such that said shared memory always contains the most recent data [(storage to a common network addressing space allowing sharing where the most updated data is always available to all nodes); abstract; Fig. 10; Col. 7, Lines 55-67; Col. 4, Lines 15-29].

Steely, Jr. fails to teach one or more cache for storing cache lines; however, teaches each processing node including buffers for storing a plurality of data to be transmitted or data received [Col. 5, Lines 24-35]. Therefore, one having ordinary skill in the art would have logically equated the cache with said buffers, as said buffers provide temporary storage for data to be transferred. Therefore, the claimed one or more caches would have been within the knowledge of one of ordinary skill in the art, as the buffers would have logically carried the same functions as the caches.

With respect to claim 45, Steely, Jr. discloses the shared memory including a first memory portion for storing unchangeable data and a second memory portion for storing changeable data [Col. 3, Line 63 to Col. 4, Line 3] and said cache coherency directory listing which node of said plurality of processing nodes have accessed copies of said cache line in said second memory portion [(control structure comprising a number of entries for a data item corresponding to number of nodes sharing the item of memory data), Col. 2, Lines 26-28].

With respect to claim 46, Steely, Jr. discloses each of said plurality of processing nodes being operable for reading, storing, and invalidating said shared memory at any other of said processing nodes [Col. 2, Lines 28-34; Col. 8, Lines 38-50].

With respect to claims 47-49, Steely, Jr. does not specifically teach accessing a second node after determining that a requested data line is not available in a first node. However, this feature would have been within the knowledge of one of ordinary skill in

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the art, as Steely, Jr. teaches maintaining coherency to allow that a request, which returns an error, would be returned by another node having the requested data [Col. 4, Line 66 to Col. 5, Line 3]. Therefore, one having ordinary skill in the art would have accessed a second node after determining that a requested data line is not available in a first node, because Steely, Jr. teaches the ability to isolate addresses being the basis for recovery from node failure.

***Allowable Subject Matter***

5. Claims 1 and 31-39 are allowed.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

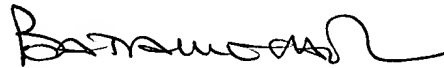
US 6,295,585 (Gillett, Jr. et al) teaching high-performance communication method and apparatus for write-only networks.

US 5,940,860 (Hagersten et al) teaching methods and apparatus for substantially memory-less coherence transformer for connecting computer node coherence domains

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Pierre-Michel Bataille  
Primary Examiner  
Art Unit 2186

March 4, 2004